
RDY
ON
ENCOMPASS ELECTRONICS (PVT) LTD.
24, West Anjaneya Temple Street , Basavanagudi - Bangalore - 560004 - India
Tel: +91 80 6522432 ; Fax: +91 4344 76322 ; E-mail: encencenc@vsnl.com
encompass

The controller – Features.

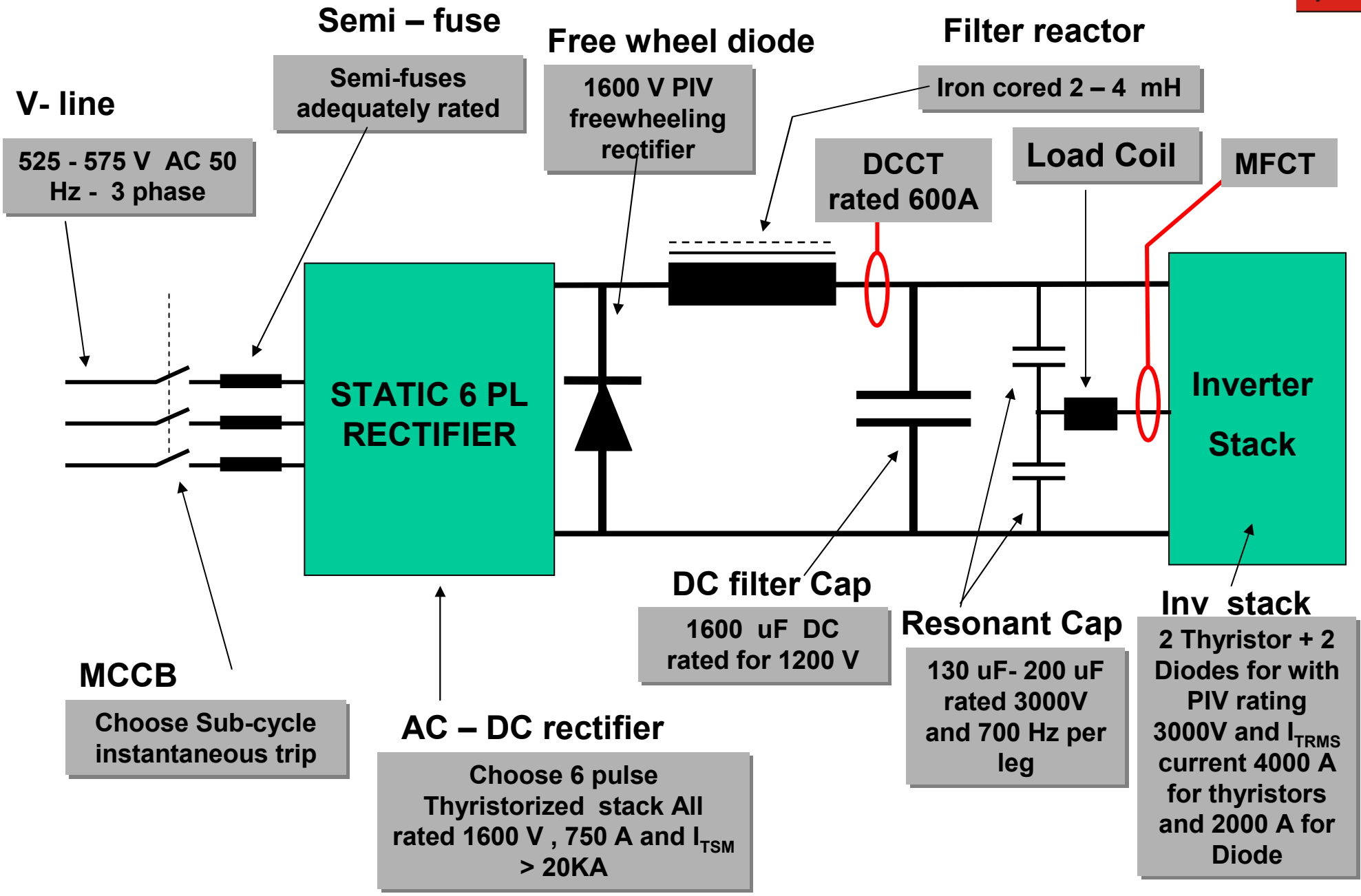
❑ 400 KW Power system configuration

- ❑ Can power AC – DC – AC resonant series high power inverters up to 450 KW.
- ❑ An AC – DC conversion in the front end is suggested to be designed with a AC 6 pulse static thyristorized switch with 6 thyristors and free wheeling diode adequately cooled.
- ❑ For thyristor based front end units use high speed sub-cycle interrupting MCCBS (Merlin Gerin type) of KA rating above 40 KA when semi-fuses are not feasible.

❑ Controller Card features

- ❑ Basic resonant inverter control circuitry.
  - ❑Build around an ASIC chip to vary resonant inverter frequency from 200 Hz to 1250 Hz.(Change Inverter control crystal U17 to 44 Mhz to get 2500 Hz)
  - ❑Basic power electronic system protection interface with LCD display module.
- ❑ AC-Static switch – controls the six front end thyristors
  - ❑ For these power units , control card comes with an additional ASIC chip one controlling the AC thyristorized static switch with 6 pulse firing with ramp up from maximum phase angle to minimum angle near 6 degree (margin)
- ❑ Maximum DC bus voltage adjustable to a fixed value and needs to be positioned so that system power factor is greater than 0.90 – 0.92.

450 KW Power circuit configuration – overall view



Recommended design approach – 1

❑ AC static switch section :

- ❑ Use 0.22 uF capacitors and 25 Ohm 100 W non-inductive resistors as sunubber circuits.
- ❑ Use MCCB with one Normally open aux contacts to sense MCCB on which will auto turn on the AC switch and soft start the DC bus to the allowed maximum voltage.
- ❑ DC reactor to be water cooled .

❑ Inverter section

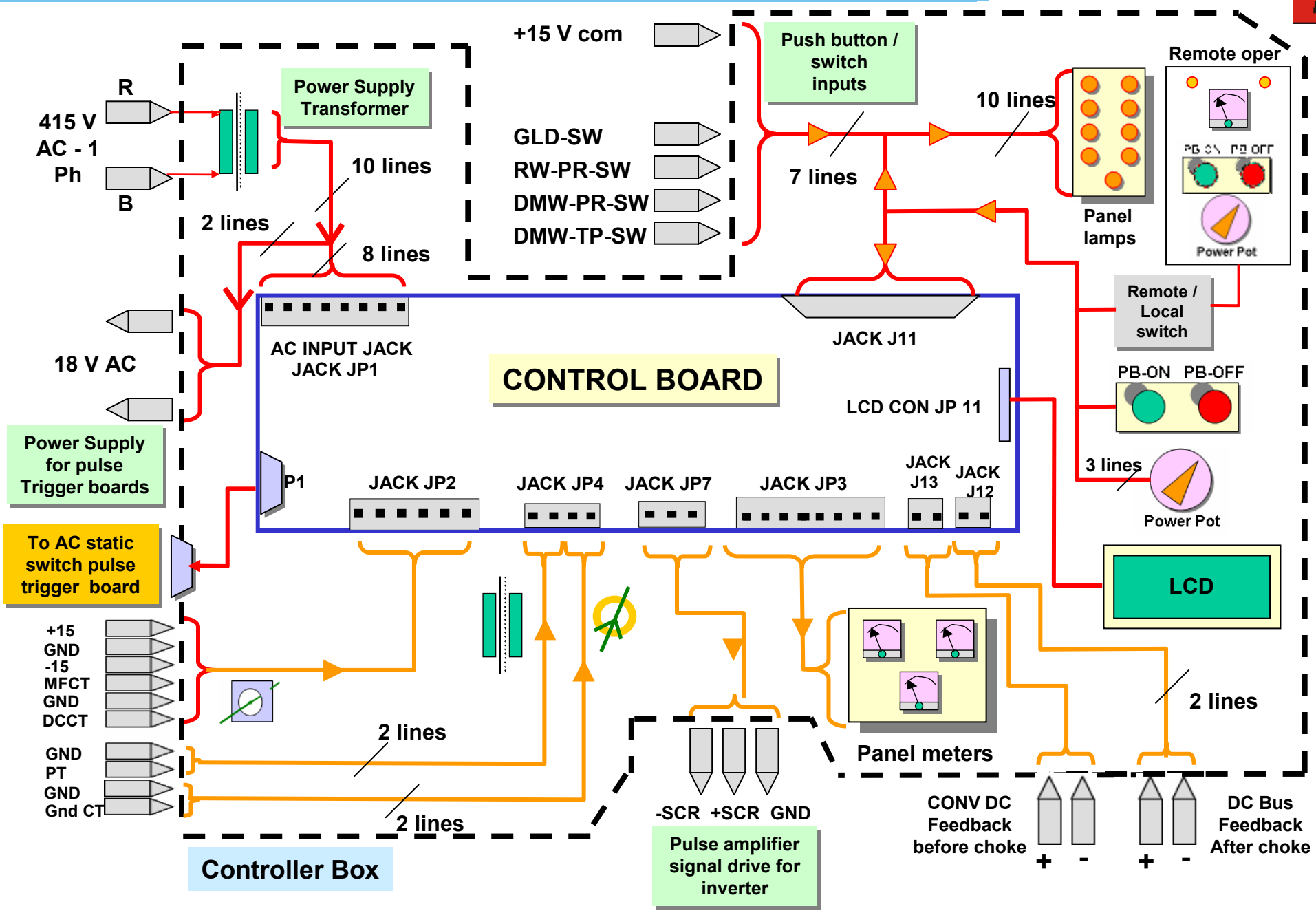
- ❑ 0.47 uF capacitor with 10 Ohm 750 W water cooled resistor as snubber components on each thyristor(Can alternatively choose the diode based snubber)
- ❑ MF CT to be rated as 5000 A / 1 A for inverter current sensing.
- ❑ Locate DI / DT coils adequately far away from MS metal components of the panel.
- ❑ DI / DT coil section to be water cooled and capable of carrying the full rated 4000 A of the inverter current.

Recommended design approach – contd

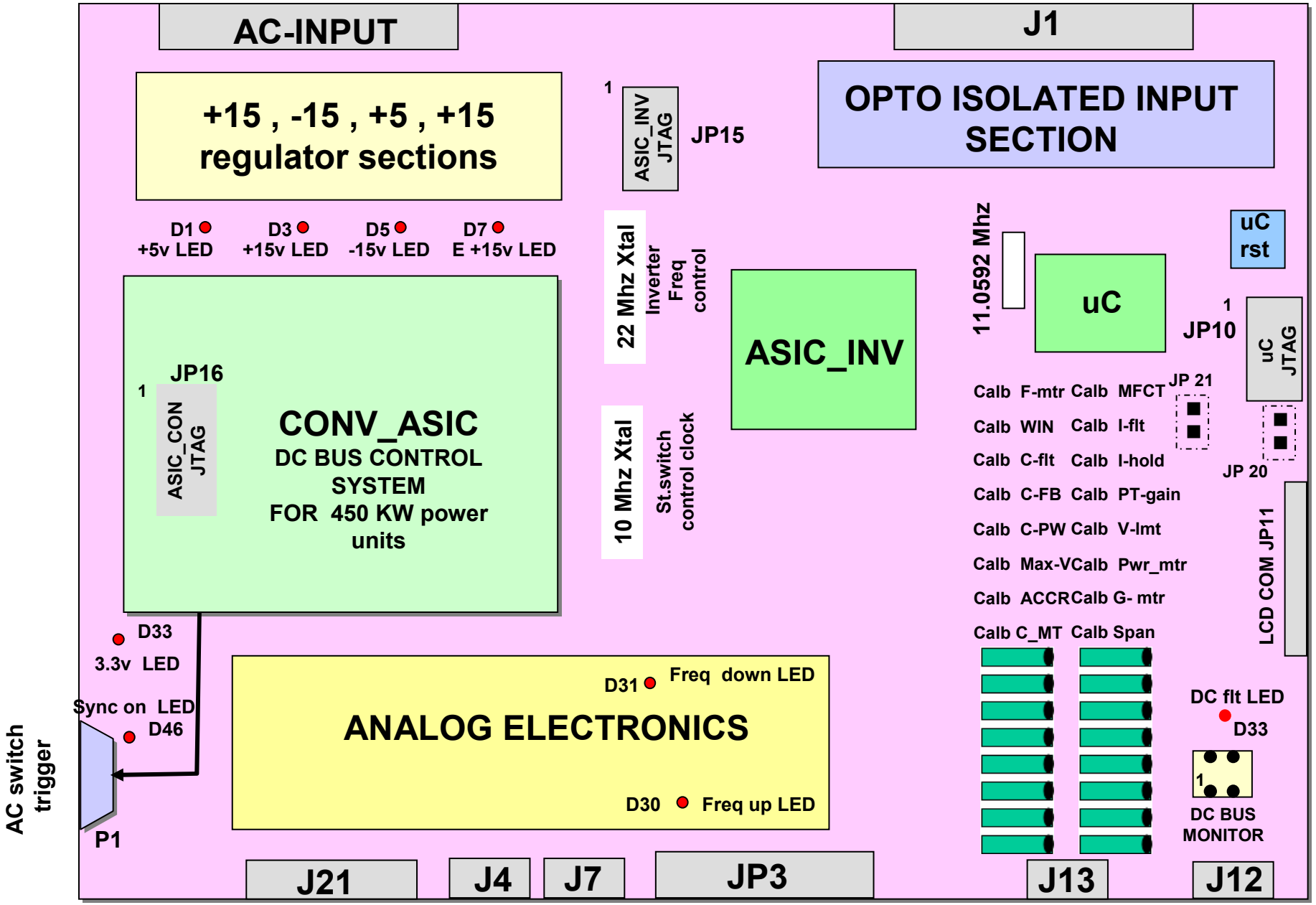
❑ Inverter Design philosophy

Series capacitor per leg	:	130-150 uF rated 3000 V rated 700 Hz. Cap 4250 KVAR / 700 Hz / 3000 V YEsha or 5450 KVAR / 700 Hz / 3000 V GE.
DC bus capacitor	:	1600 uF rated 1200 V
Incoming AC voltage	:	415 - 525 V ac three phase with Converter 6 pulse soft start with free wheeling diode .
Furnace coil	:	27 turns , Diameter 650 mm , Height 785 mm Coil measure inductance (320 uH) D^2/L = 0.0.538 Expected operating freq at peak power 550 Hz.
Actual measured oper. Char	:	3000 V on inverter. (600) A on lines = 450 KW. Operating frequency at peak power 600 Hz. Jumbo C770 inverter SCR and matching diode
DI/DT coil	:	12 uH per leg

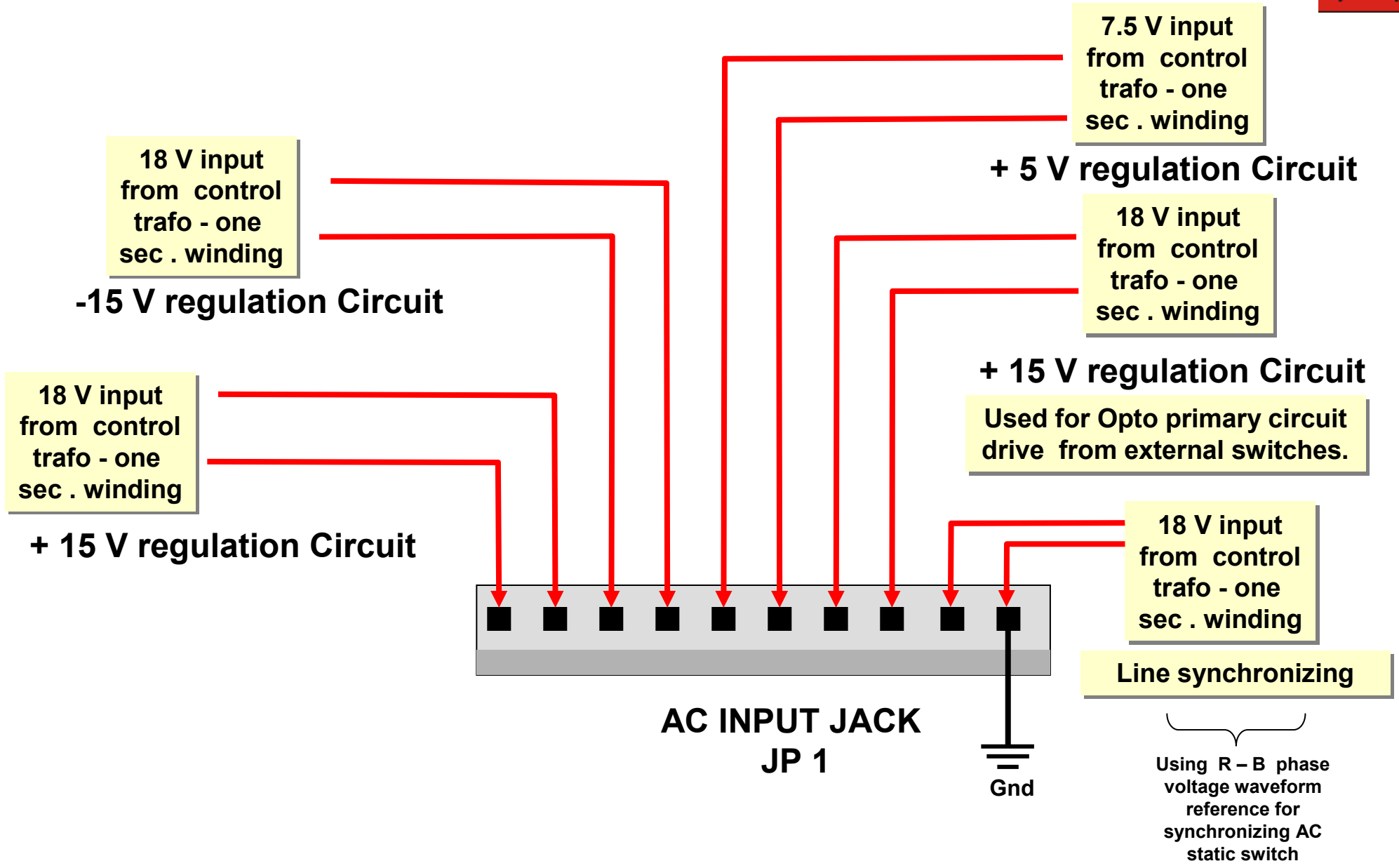
The controller wiring scheme



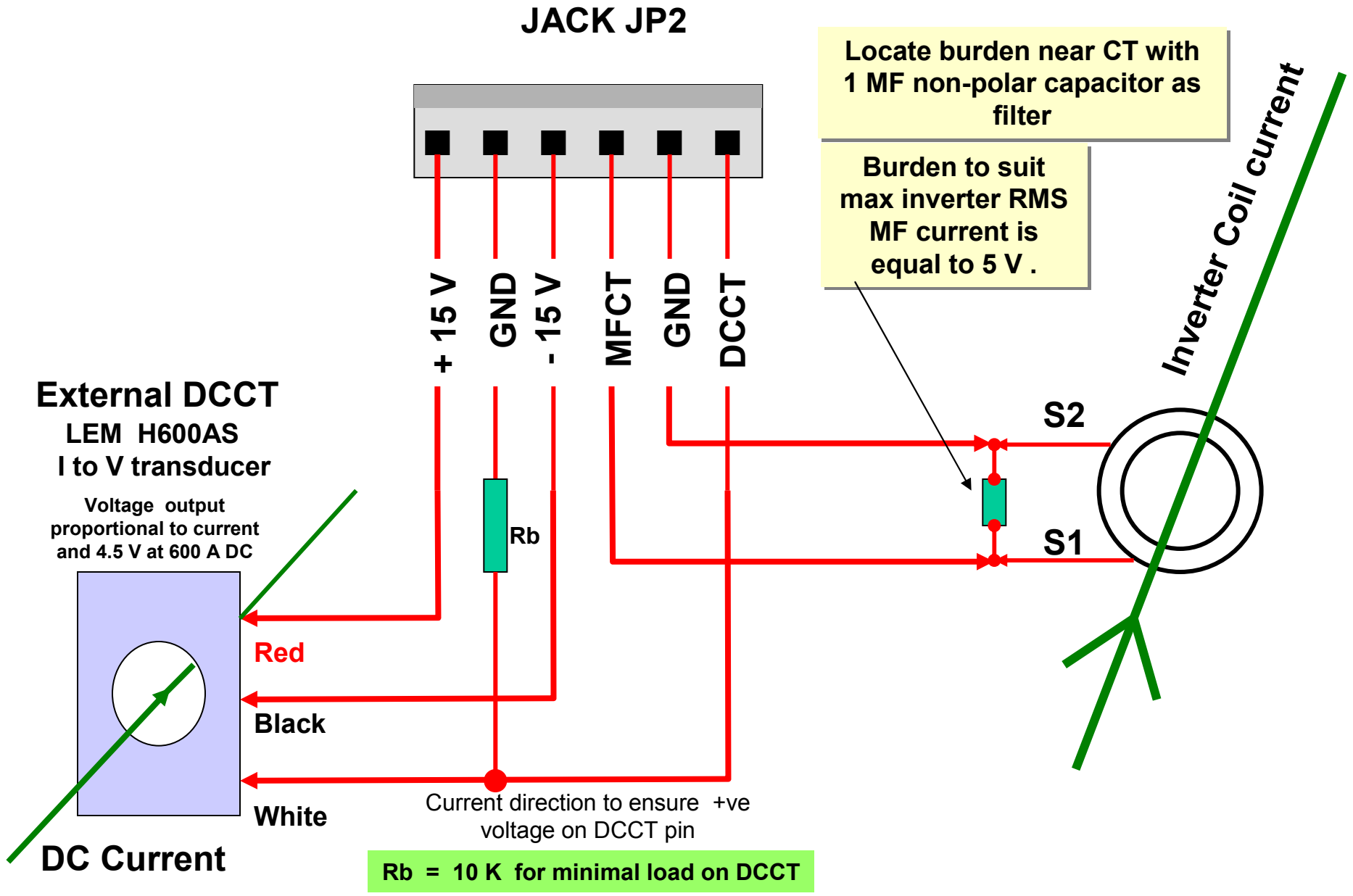
Control board layout.



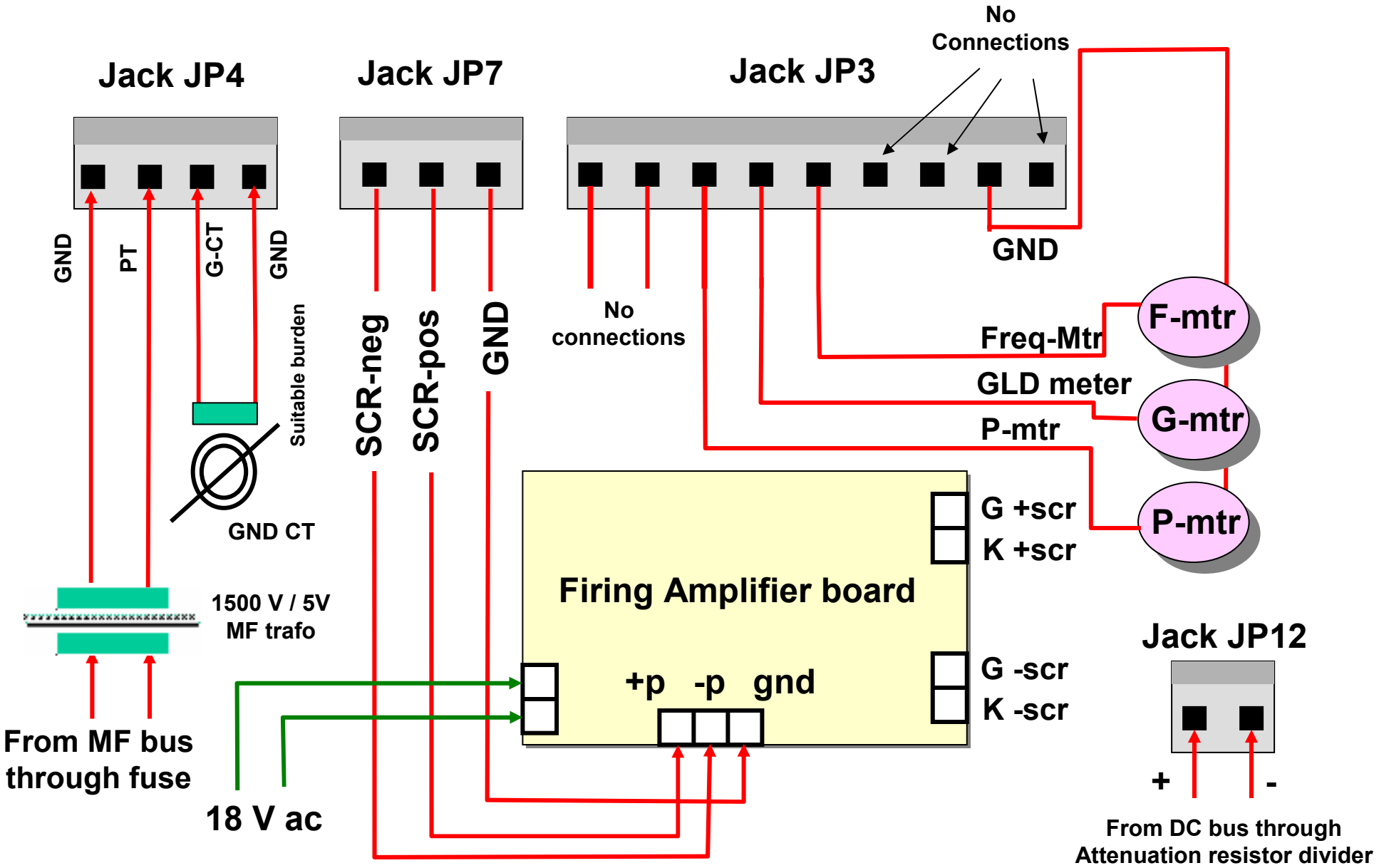
Jack AC-INPUT for ac voltages input for regulator.



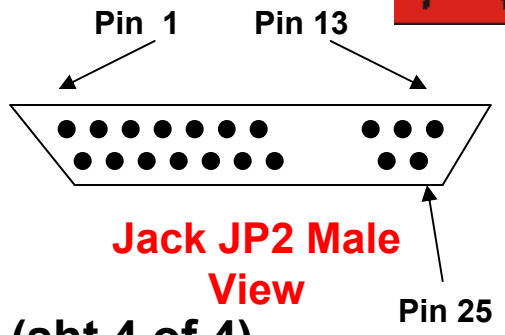
Jack JP2 for CT inputs and control connections.



Jack JP4 , JP2 , JP7 , JP12 & JP3 connections.



Jack JP2 - D25 pin_outs for Lamp drives & inputs



Pin : 13 ..... + 5 V (ASIC supply) .
Pin : 12 ..... OC- FLT lamp. .....
Pin : 11 ..... INV_ON lamp. .....
Pin : 10 ..... RDY lamp. .....
Pin : 09 ..... DMW-PR lamp. .....

From ASIC Through Buffers

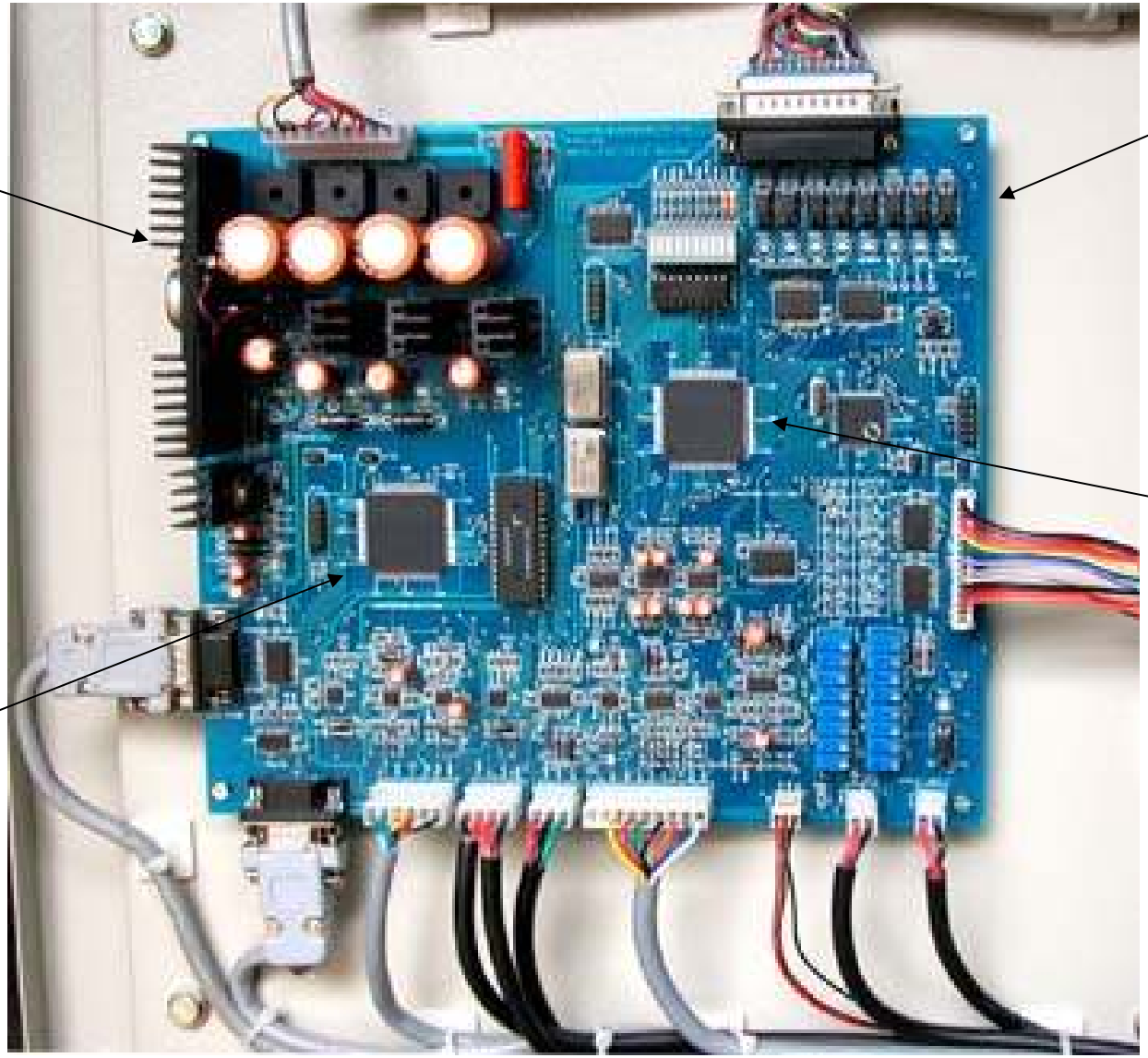
Pin : 08 ..... Pot Wiper ..... .Internal point PW (sht 4 of 4).
Pin : 07, 06 & 05 No connection.
Pin : 04 ..... OFF push button .....Drives OFF-PB opto (sht 4 of 4).
Pin : 03 ..... GDL-trip input ..... Drives GLD opto (sht 4 of 4).
Pin : 02 ..... DMW-temp input ..... Drives DM-TMP opto (sht 4 of 4).
Pin : 01 ..... Gnd (Electronics inputs +15 V gnd) (opto primary circuit).
Pin : 25 ..... DMW-TEMP lamp. .....
Pin : 24 ..... DC_FLT lamp. .....
Pin : 23 ..... HOLD lamp .....
Pin : 22 ..... RW-PR lamp .....

From ASIC Through Buffers

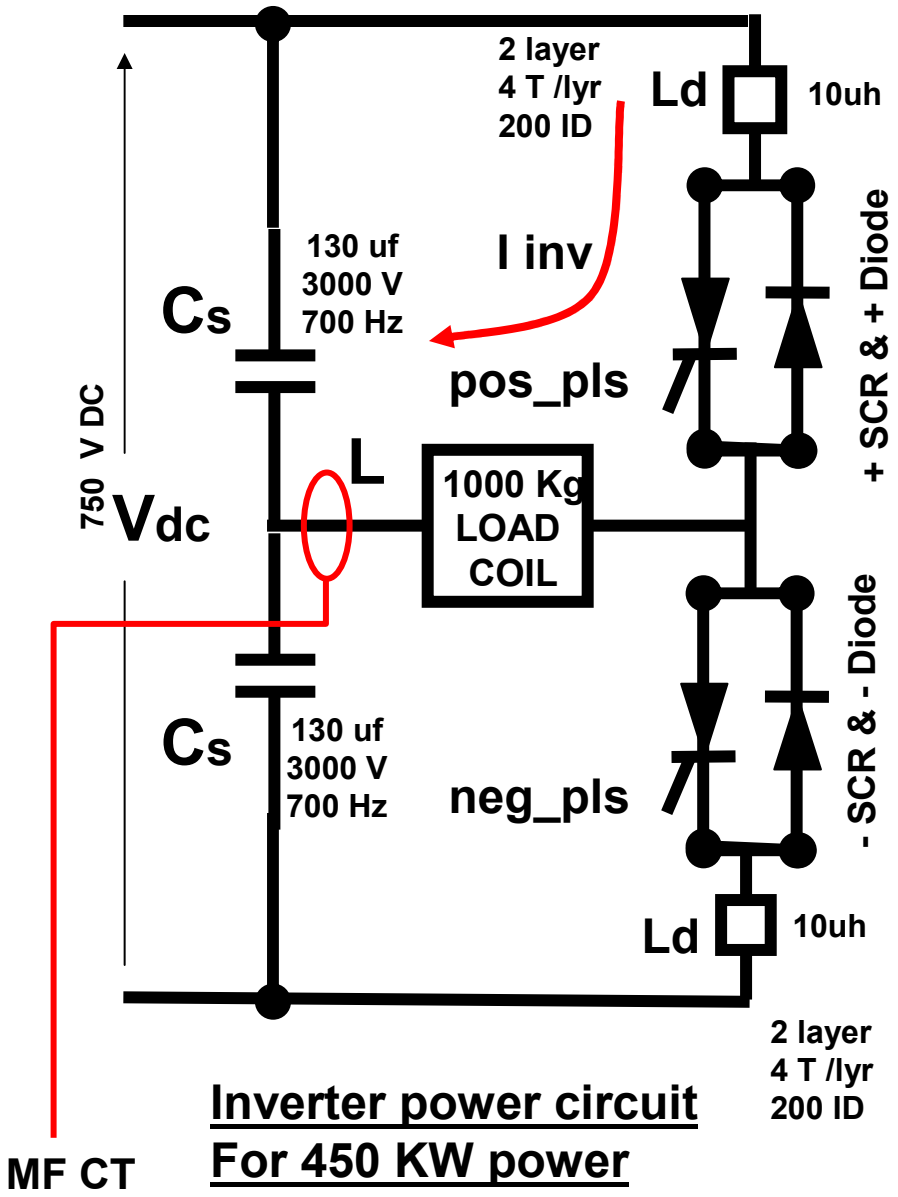
Pin : 21 ..... POT HI-END ..... Internal point PH (sht 4 of 4).
Pin : 20 ..... POT LO-END ..... Internal point PL (sht 4 of 4).
Pin : 19 & 18 No connection.
Pin : 17 ..... ON push button ..... Drives ON-PB opto (sht 4 of 4).
Pin : 16 ..... RW-PR input ..... Drives RAWPRIP opto(sht 4 of 4).
Pin : 15 ..... DMW_PR input ..... Drives DMPRIP opto (sht 4 of 4).
Pin : 14 ..... +15 - Electronics input -OPTO primary side use & PWR_ON lamp.

View of wired control card on typical 100 KW unit

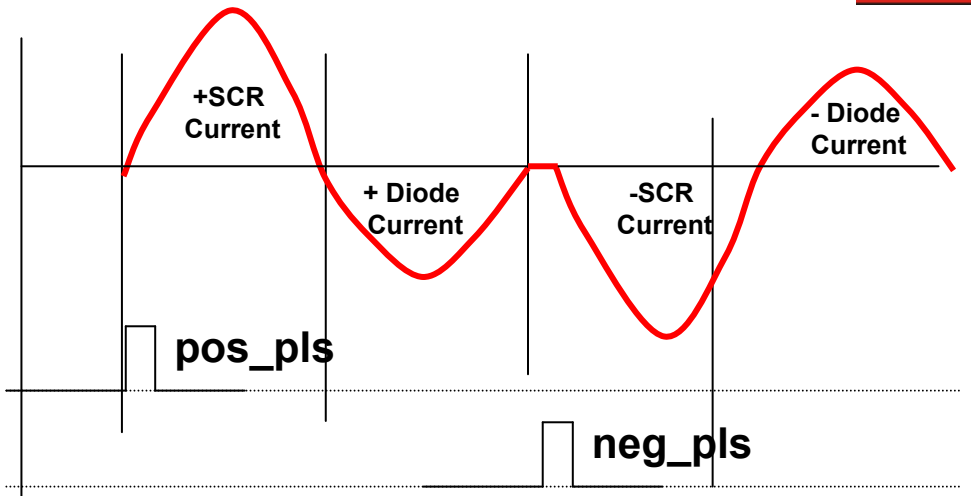
- Illustration for card with AC static switch control



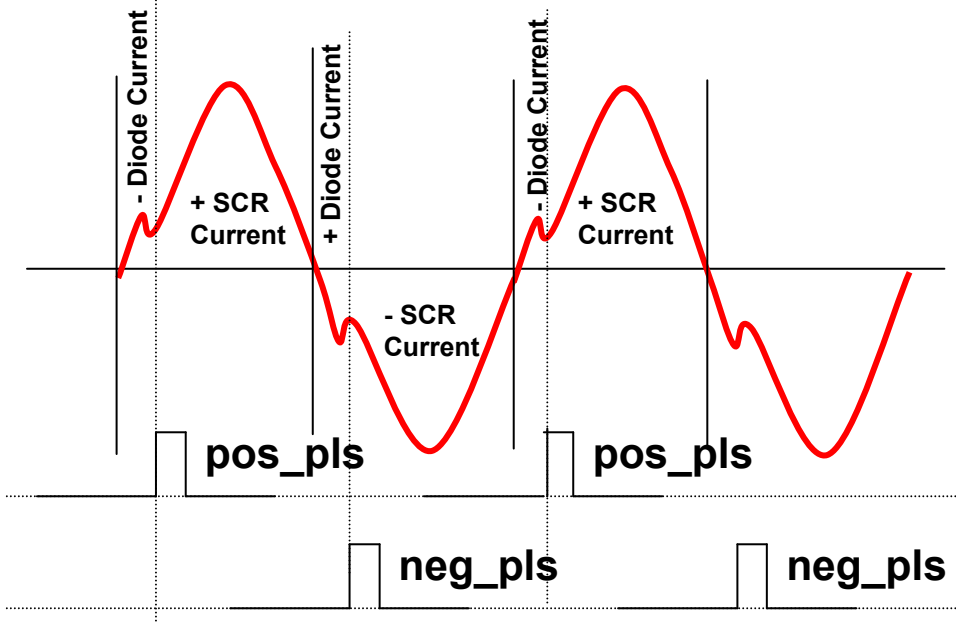
Power circuit response to the control system.



Inverter power circuit
For 450 KW power

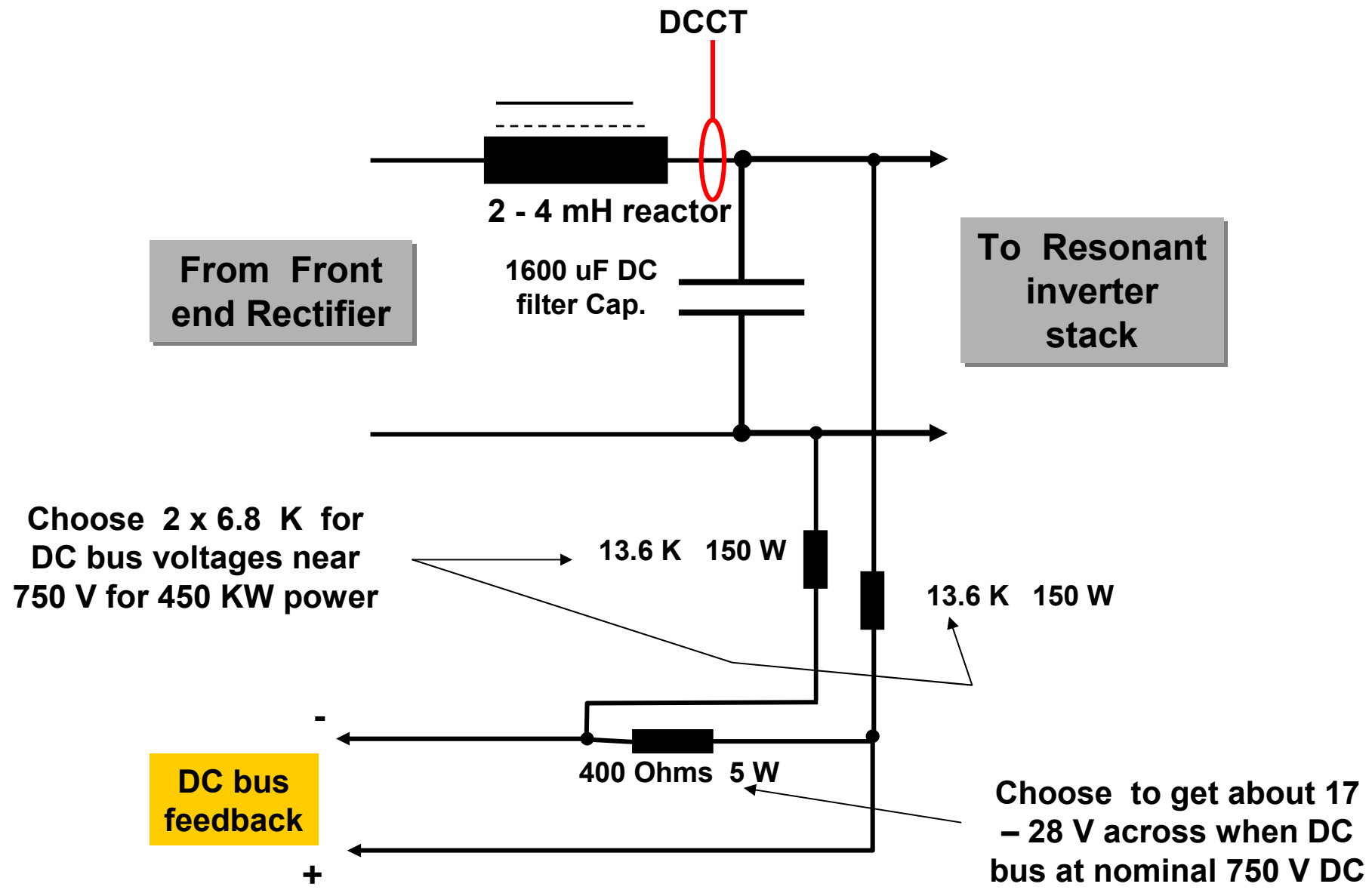


LOW FREQ operation without overlap



HIGHFREQ operation with overlap

DC bus feed back for Inverter protection



Connection scheme – rear of controller

18 V AC Power supply for Inverter firing board unit comes from here .

Use shielded cable to connect Inverter thyristor firing board here

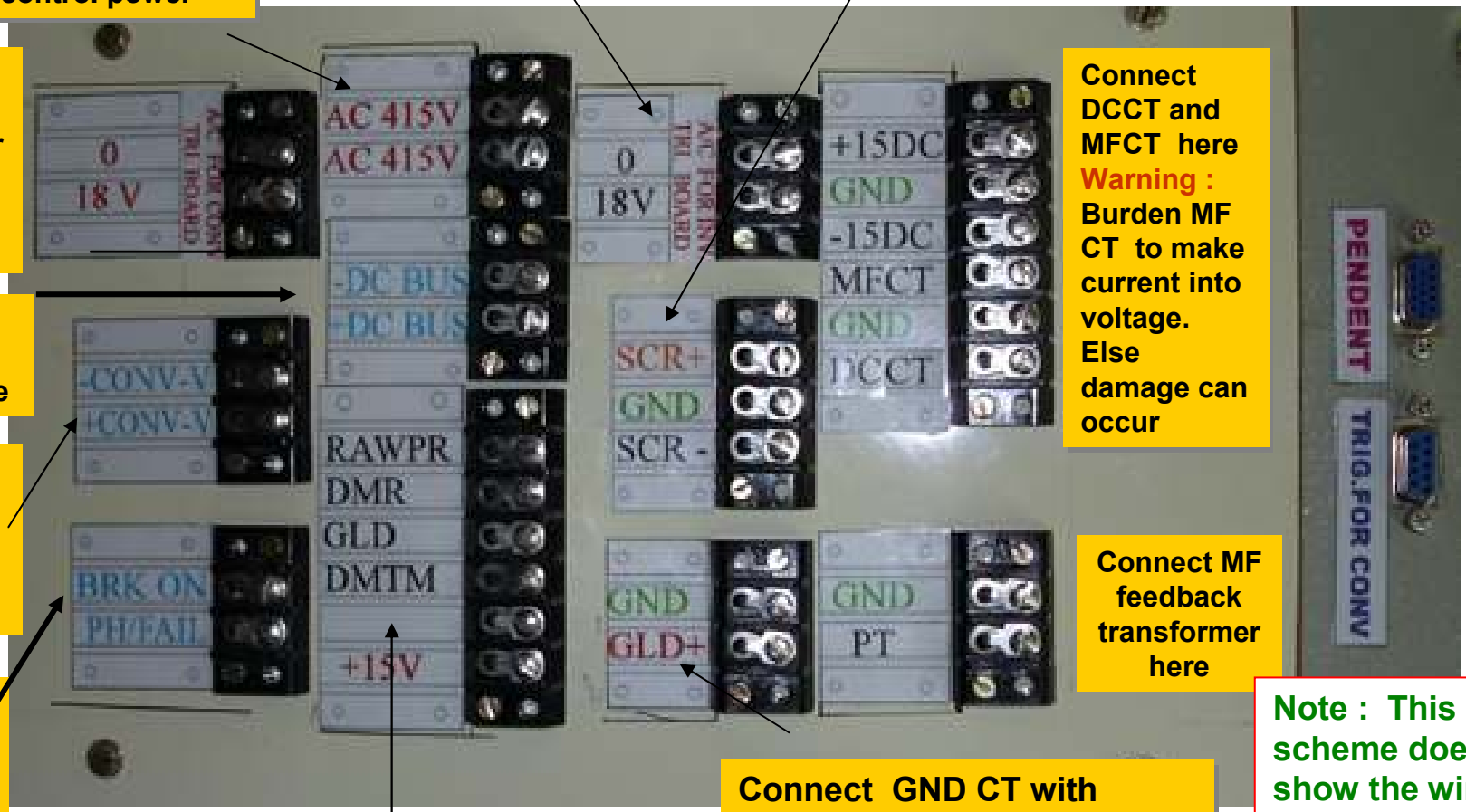
415 control power

18 V AC Power supply for conv firing board

DC bus feedback after choke

CONV output feedback before DC choke

NO contact from incomer MCCB to auto start DC bus



Connect DCCT and MFCT here
Warning : Burden MF CT to make current into voltage. Else damage can occur

Remote on/off pendant

STATIC SWITCH trigger

Connect MF feedback transformer here

External interlock & protection . Use NC contacts

Connect GND CT with burden to convert to voltage.
Warning : Usage without burden will damage unit

Note : This scheme does not show the wiring for the AC static switch firing and remote on / off unit

Front facia of controller

Operating Inverter Frequency

Operating power

Blinking light when system ready. During fault condition shuts off

Turns on when inverter turned on

Max Voltage or power lamp

Illuminates when DC bus collapses.

Inverter ON PB

Ground leakage meter

External power applied lamp

Power set potentiometer

Inverter Over current or ground fault

Raw water pressure interlock (use NC)

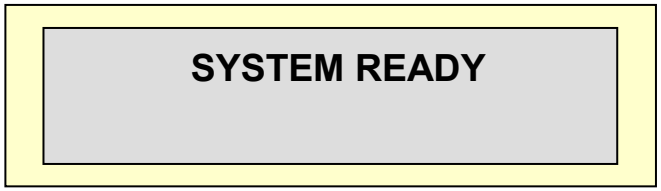
DM water pressure interlock (use NC)

DM water temperature interlock (use NC)

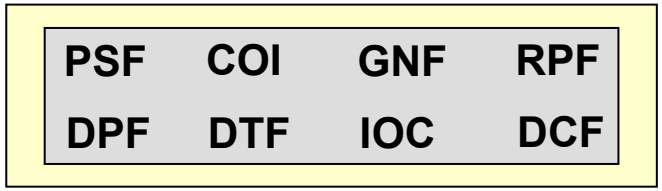
Inverter OFF PB

LCD digital display and settings – 1

- Displays running parameters in percentage from 0 to 100 %
- Fault indications & display controlled from micro controller. Use ***uC rst*** switch for resetting micro controller is case of corrupted display. Resetting micro controllr has no effect on inverter / static switch control systems.
- Card adjustment potentiometer settings using JP20 and JP21
  - Normal operation : JP20 is in place.
  - Calibration of card setting : JP21 - Page 1 of setting .
    JP21 & JP 20 - Page 2 setting .
- LCD display conditions



System ready for switch on



Fault in system

PSF : Phase sequence Fail – (units with AC switch control)

COI : Converter over current - (units with AC switch control)

GNF : Ground fault. Sensing from external Ground leakage detector.

RPF : Raw water Pressure Fault from external NC interlock.

DPF : DM water pressure –ext interlock

DTF : DW water temp – ext interlock.

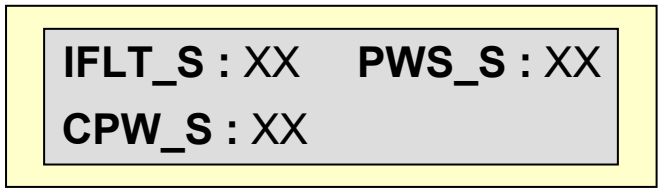
IOC : Inverter over current

RPF : DC bus fault

Fault reset is by pressing the OFF PB.

LCD digital display and settings – 2

- Displays calibration settings of potentiometers on card.
  - All settings as nominal 100 % maximum.
  - Display organized as two pages .
    - Page 1 display when JP21 is shorted.
    - Page 2 display when JP21 and JP 20 are shorted .
    - Normal running condition is when JP 20 is shorted.

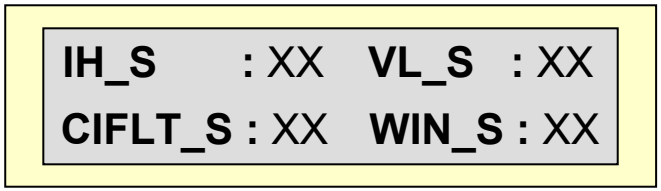


Page 1

IFLT_S : R15 IFLT (TP 10) CW increase (refer DWG sheet 2 of 9)

CPW_S : R170 MAX V CW increase (refer DWG sheet 9 of 9)

PWS_S : R59 SPAN CW increase (refer DWG sheet 3 of 9)



Page 2

IH_S : R22 IHLD (TP 11) CW increase (refer DWG sheet 2 of 9)

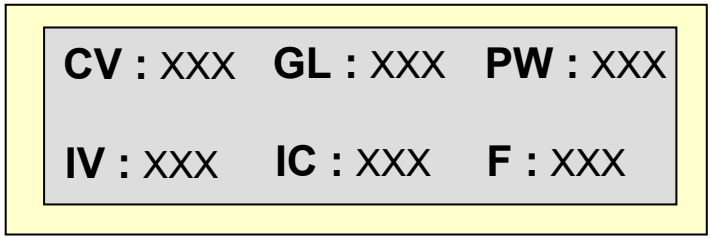
VL_S : R41 VLMT (TP13) CW increase (refer DWG sheet 2 of 9)

CIFLT_S : R123 CFLT CW increase (refer DWG sheet 3 of 9)

WIN_S : R63 WIND CW increase (refer DWG sheet 3 of 9)

LCD digital display and settings – 3

- Display when system in operation



Fault in operation

CV : Converter voltage in 0 to 100 %

GL : Ground leakage current in 0 to 100 %

PW : Power level 0 to 100 %

IV : Inverter voltage 0 to 100 %

IC : Inverter current 0 to 100 %

F : Frequency 0 to 100 %

Trigger signals STATIC SWITCH CONNECTION

- The firing signals for Static switch SCRs from Trigger board

R-P SCR : R phase positive SCR

Y-P SCR : Y phase positive SCR

B-P SCR : B phase positive SCR

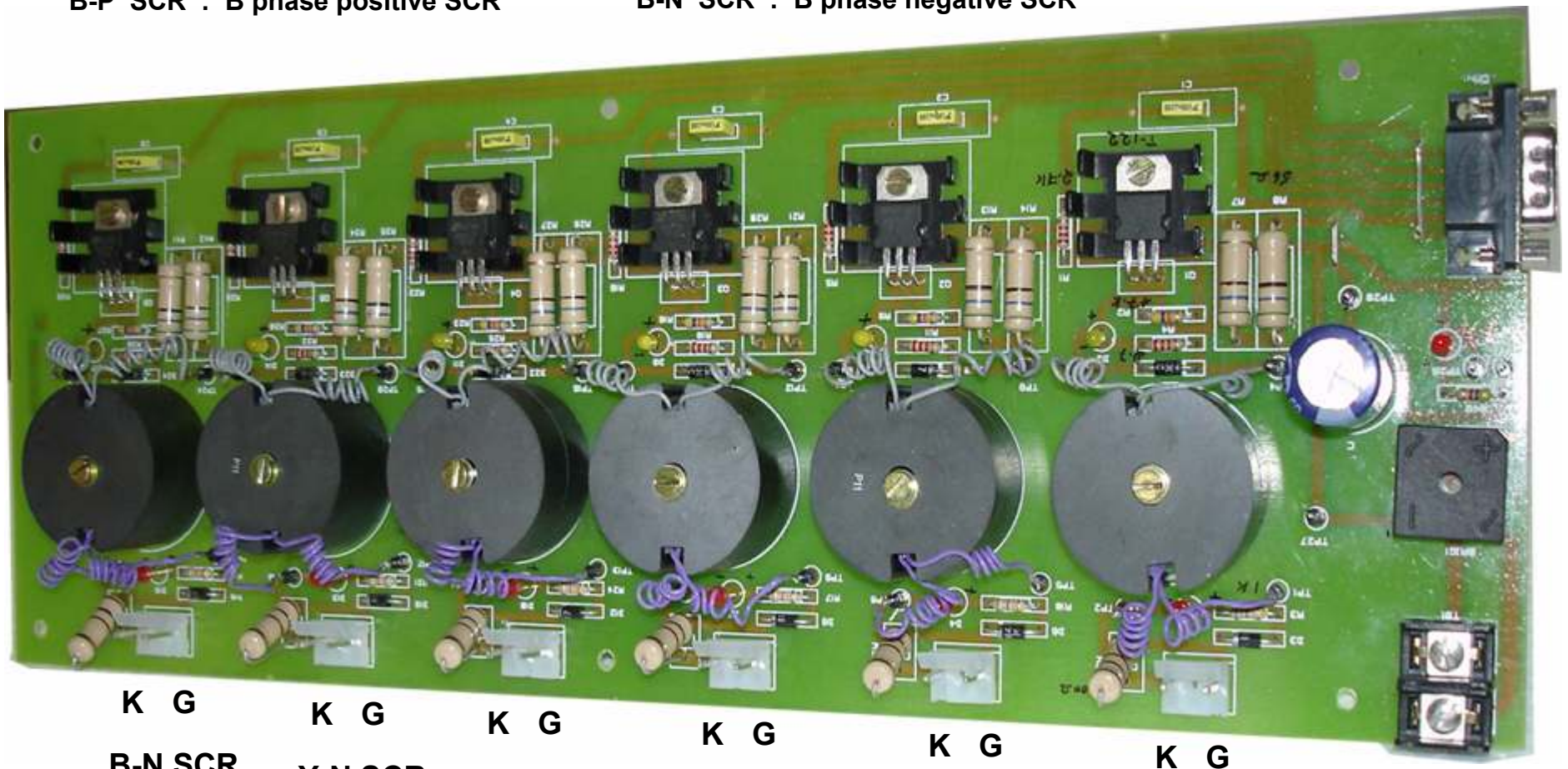
R-N SCR : R phase negativeSCR

Y-N SCR : Y phase negative SCR

B-N SCR : B phase negative SCR

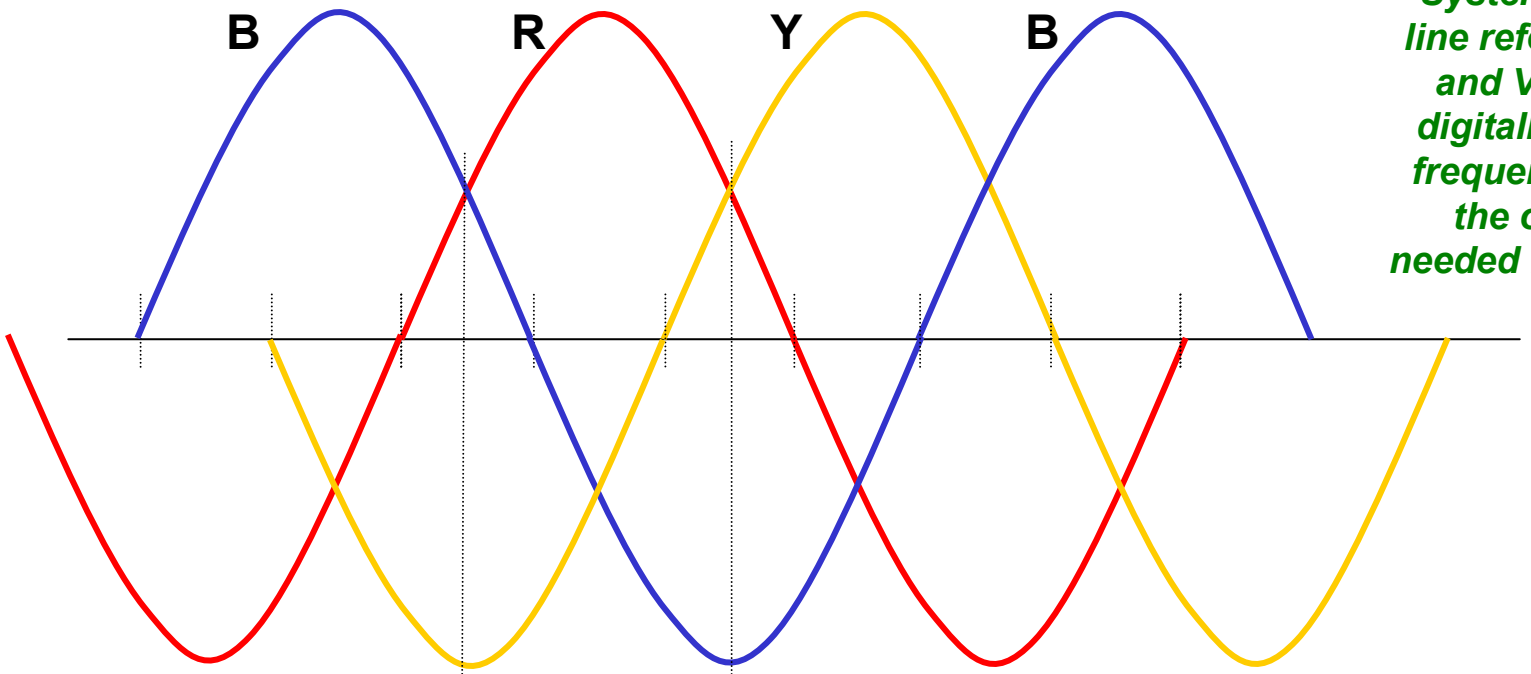
G : gate

K : Kathode



Synchronizing the STATIC SWITCH

- The procedure
  - Uses the AC 18 V synchronizing waveform in JP1 jack (refer page 8)
  - This synchronizing voltage should be ***V_{RB}*** (R phase to B phase 415 volts)
  - Illustration for the R + SCR (similar for the other five SCRs)



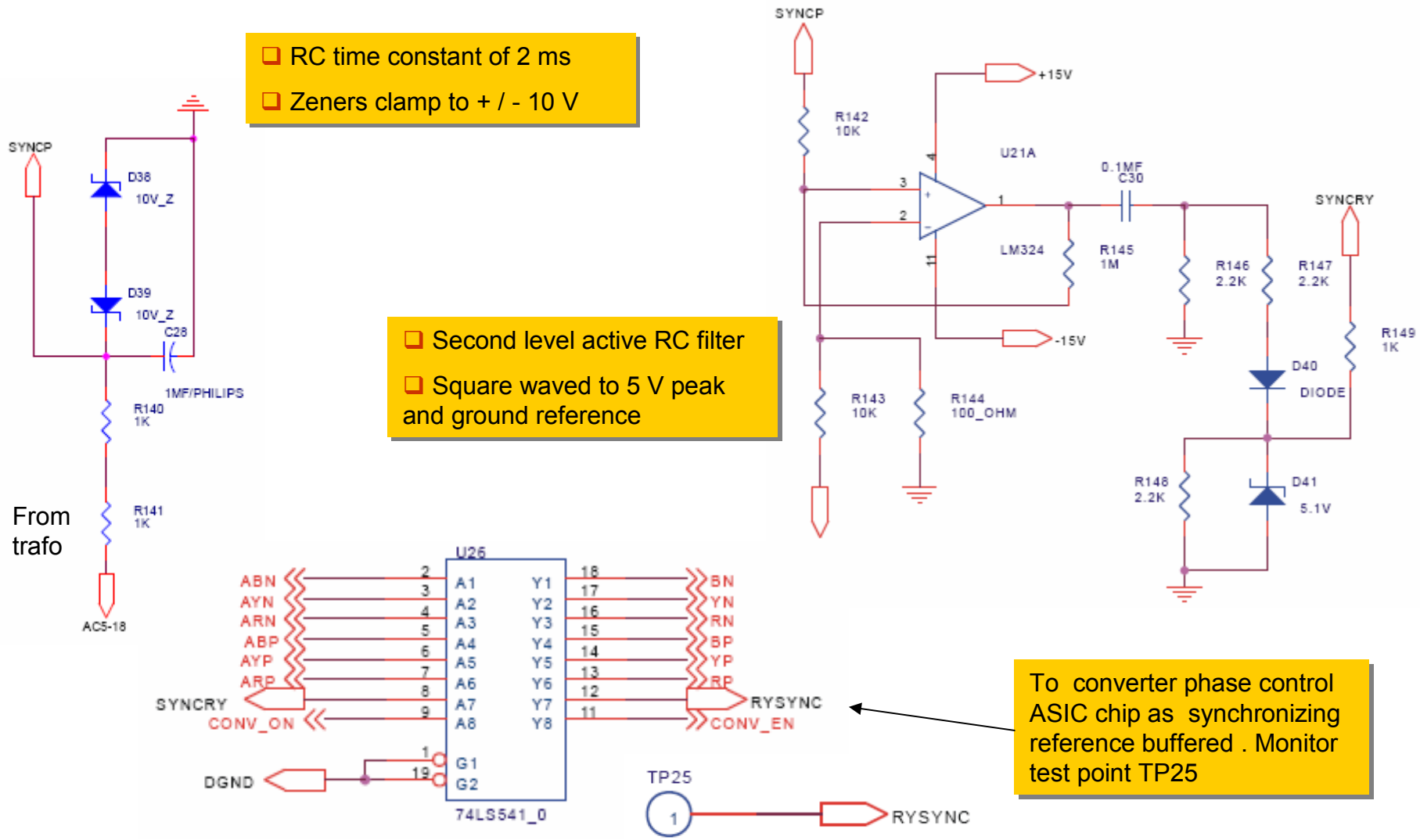
System uses one line to line reference between V_R and V_B and internally digitally locks to the line frequency and generates the other references needed for all the other five SCRs.

Circuit design notes – 1

- Synchronizing input from transformer RC smoothening , filtering & clamping
  - **AC5-18 → SYNCP → SYNRY → RYSYNC**

- RC time constant of 2 ms
- Zeners clamp to + / - 10 V

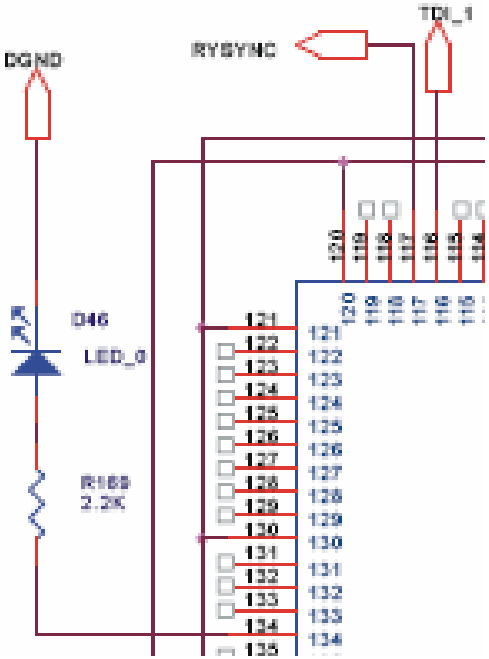
- Second level active RC filter
- Square waved to 5 V peak and ground reference



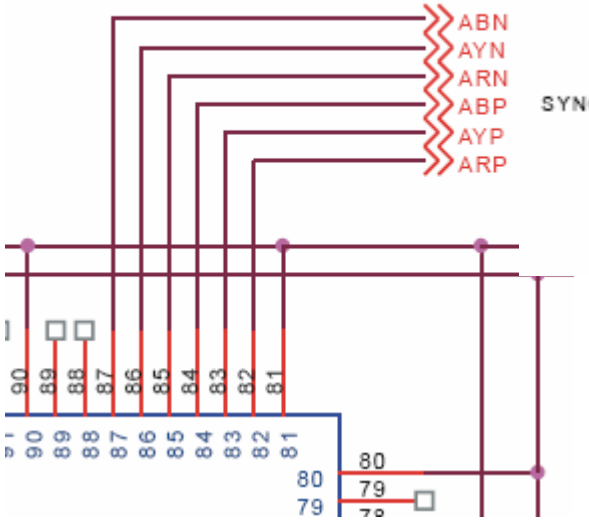
To converter phase control ASIC chip as synchronizing reference buffered . Monitor test point TP25

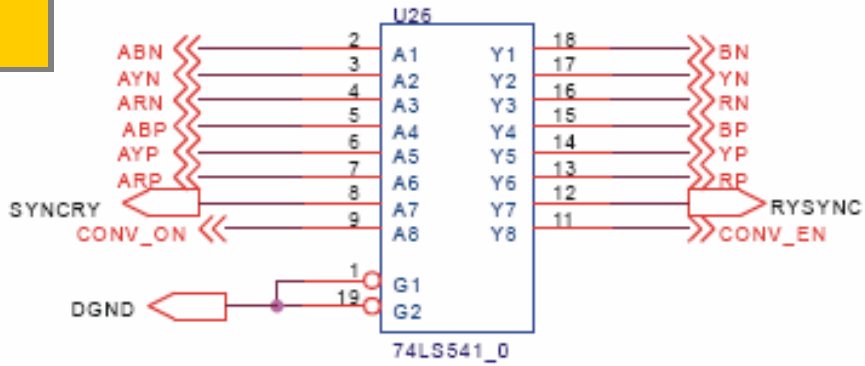
Circuit design notes – 2

- Converter Thyristor Gate trigger outputs - six signals generated by ASIC
  - **RP , BN , YP , RN , BP , YN** is the sequence when RYP is the line sequence



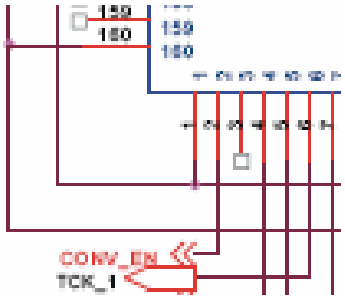
- Six firing pulse signals from the ASIC – Pins 81 → 87



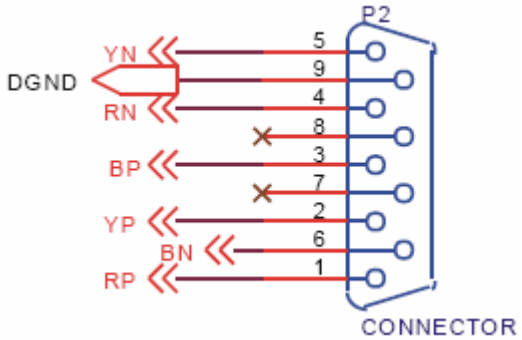


- All six pulses buffered.
- CONV_ON signal from Inverter ASIC which senses Breaker_on signal .

- Sync signal at pin 117
- ASIC produces sync capture signal at pin 124 tied to LED 46 indicator
- Pulse signals enabled by CONV_EN signal



- Test point TP 24 for RP pulse
- Test point TP26 for 60 deg pulse train



- All six pulses brought out to connector

Notes on synchronizing

- Reversal of the VRB in synchronizing will prevent the DC bus from turning on.
  - This can be identified that the DC bus will not soft start to the maximum DC voltage adjusted with R 170 potentiometer.
  - Best way to check synchronization is to use two 100 W lamp loads in series across the DC bus and see soft start. If VRB is not correct soft start wont happen and the lamps will momentarily blink and disappear. If no lamp load is available this can be identified that the DC voltmeter in the panel will not rise slowly but momentarily the DC cap bank will charge up and hold max voltage.
  - DC bus soft starting and under control of R170 potentiometer is conclusive in showing that synchronizing is perfect.
  - Ensure that there is a small bleed in the DC bus (The DC bus monitor resistances of 6.8 K used normally will be sufficient - page 14)

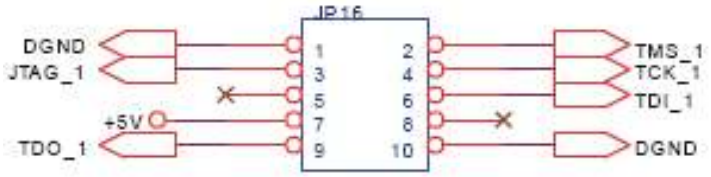
- Unit has over-current trip on the AC static switch. Hence any very high starting surge current during start up (or failed DC bus capacitor) will cause Converter Over Current fault in controller and indicated by bthe OC-FLT fault lamp coming on and COI fault in display

- Static switch will auto start when Line breaker is closed and detected by the auxiliary NO connection at “BRK ON“ connected to +15 V (see page 15)

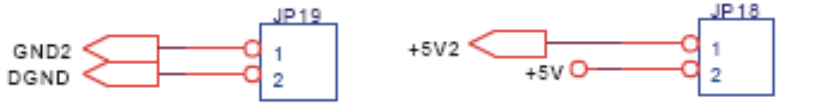
- The Phase fail connection (page 15) can be used for interlock if external Phase reversal / fail detector circuit / instrument is used externally . This controller has no facility to detect phase fail or reversal.

Circuit design notes – 3

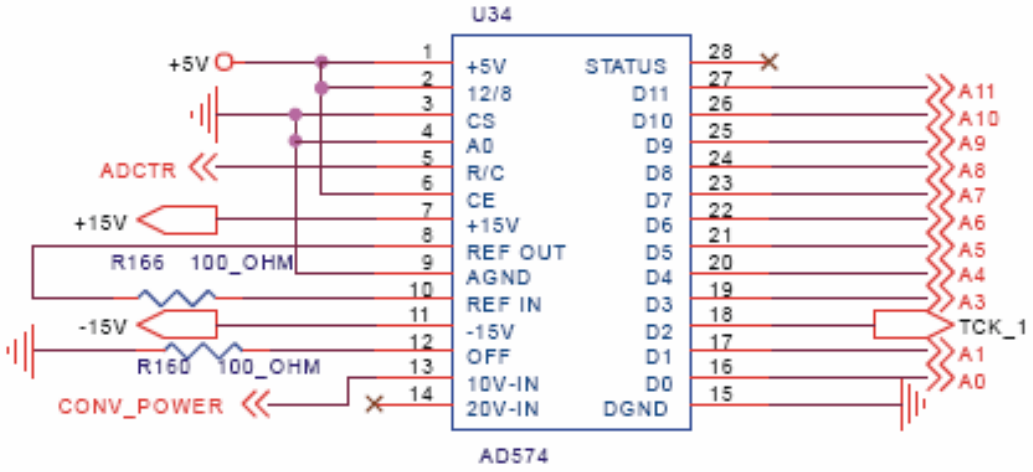
- Notes on Converter Thyristor Gate trigger ASIC .
  - Power supply +5 v and GND through jumpers JP18 & JP19.
  - ASIC control program connector JP18 for program download .
  - U16 Converter control Crystal (10 Mhz) controls all internal control processes .
  - ADC chip U34 provides analog interface for converter phase angle control analog signal conversion to digital reference (12 bit) . ADC control is through converter ASIC (pin 17 : ADCTR signal)



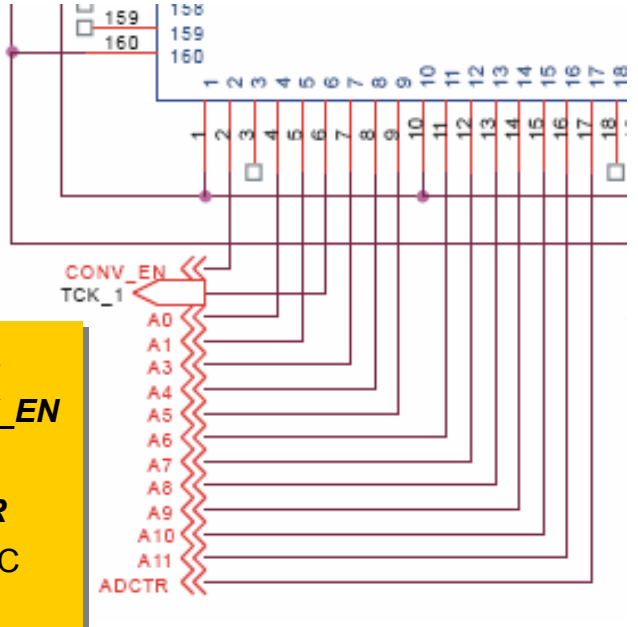
- JP16 for program download



- JP18 & JP 19 for ASIC +5 V and GND



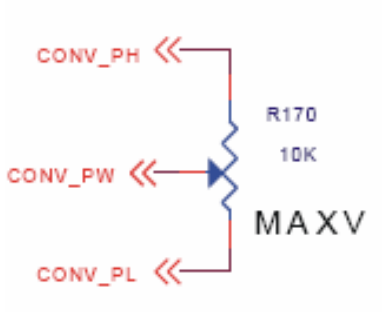
- ADC converts max 10 V-in CONV_POWER analog signal to 12 bit digital signal ***A0→A11***



- Converter ASIC enabled by ***CONV_EN*** signal fro Inverter ASIC and ***ADCTR*** signal controls ADC chip

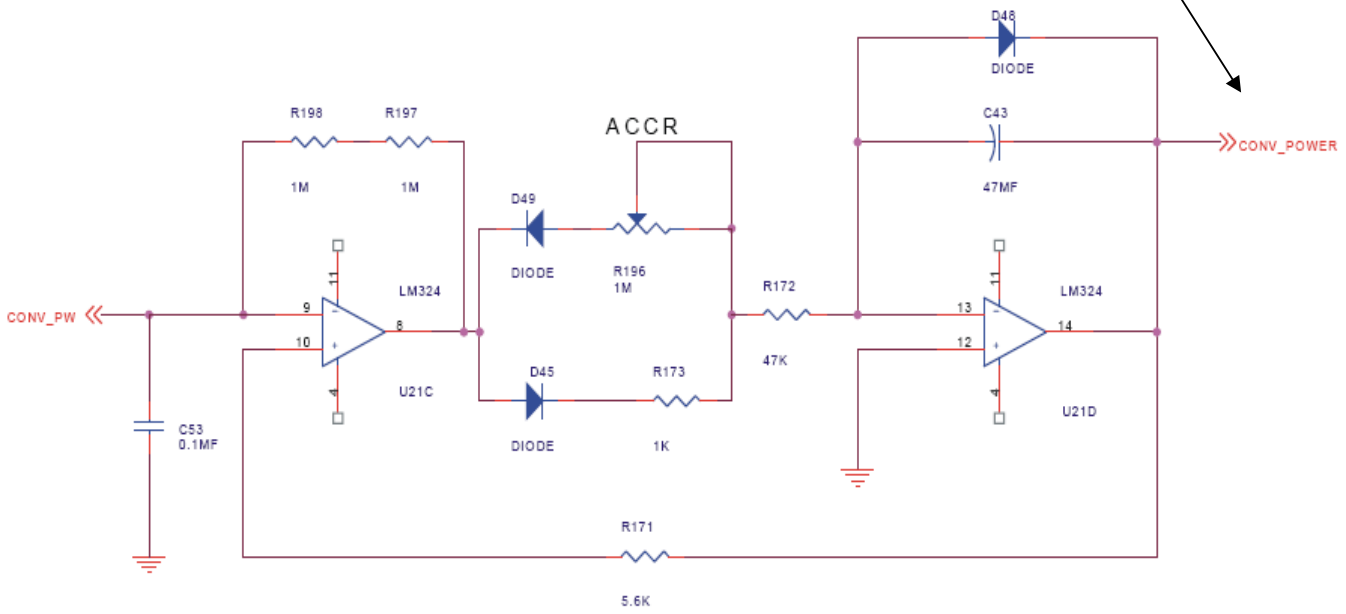
Circuit design notes – 4

- Notes on Converter min and max phase angle setting and metering and ASIC program downloading
  - Downloading connector JP16.
  - Maximum Converter Voltage controlled by pot set R170
  - U21D OpAmp circuit controls Converter phase angle ramp up speed and drop out . Ramp up adjustable (soft start) with R196 (ACCR pot)



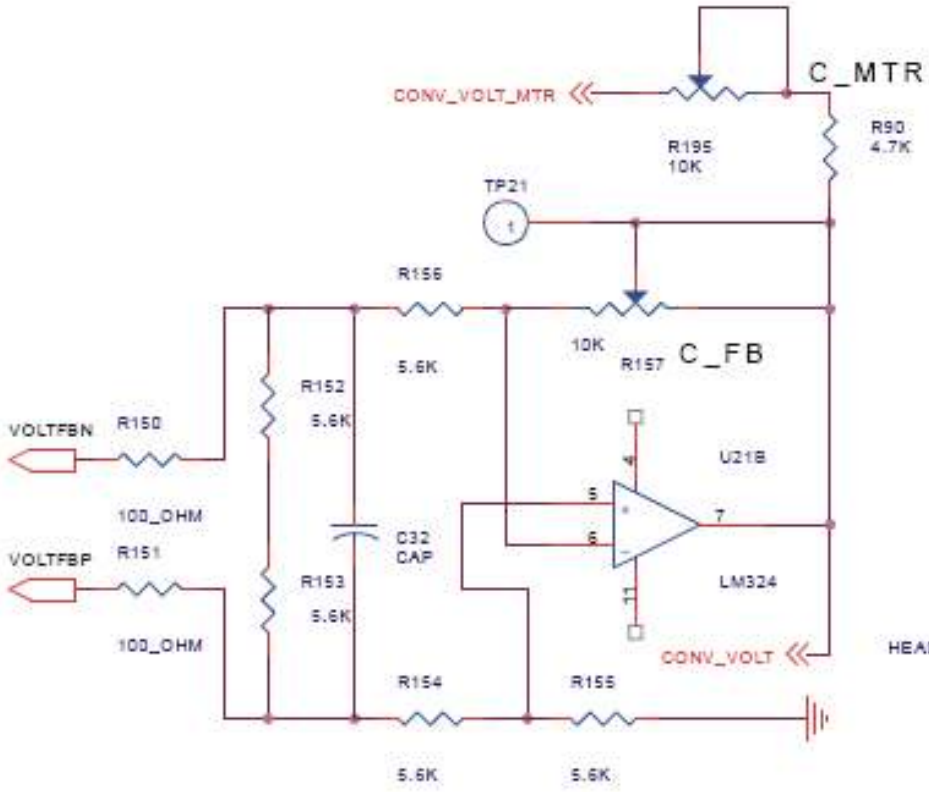
- R170 – Max Conv Volt

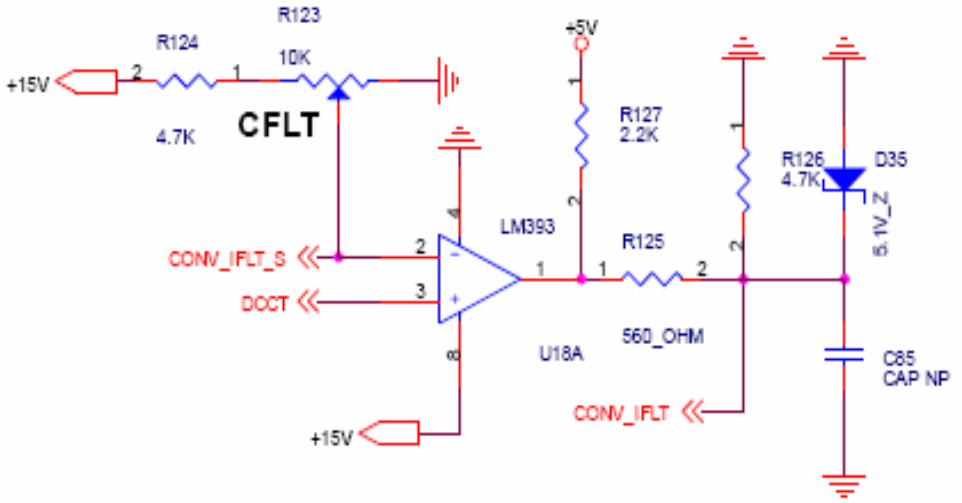
- To Pin 13 of ADC chip for converter phase angle control analog voltage for Digital conversion

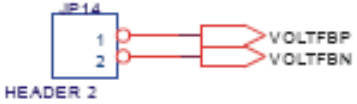


Circuit design notes – 5

- Converter over-current fault circuit and Converter volt metering circuit
  - Feed back of converter DC bus . Use 200 K 5 W drop resistor on each leg
  - DC meter calibration (1 mA fsd) with pot R195 (C_MTR) and or R157 (C_FB)
  - DC current DCCT sense compared for setting converter fault (R123 – CFLT pot)





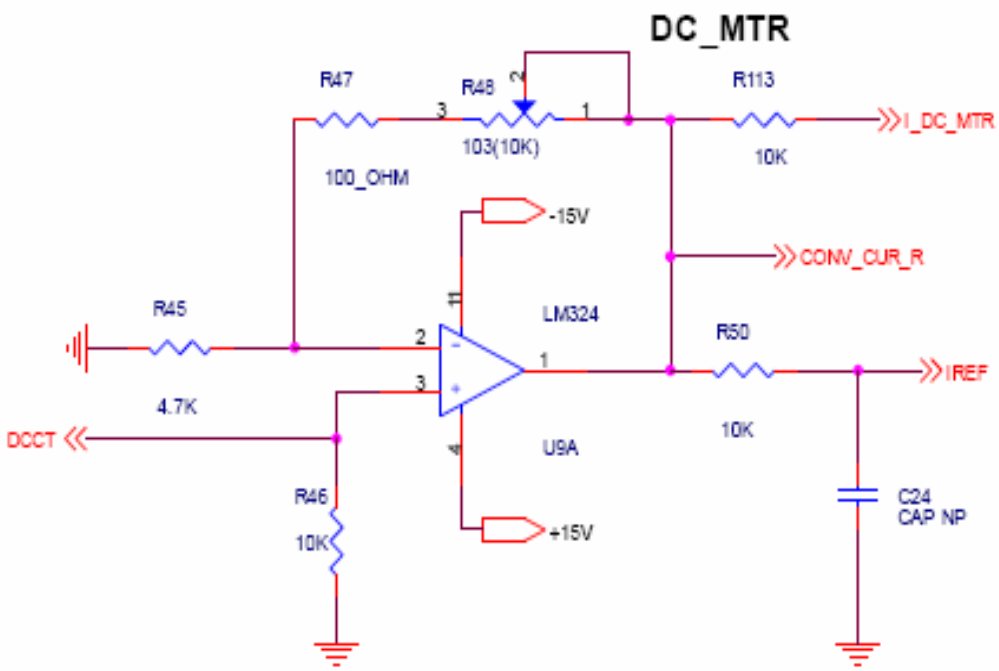


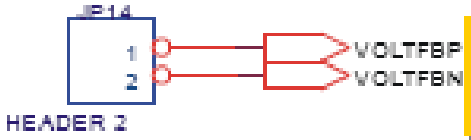
- Connect to DC bus through 200 K , 5 W resistor

- U18A comparator for CFLT – Converter over current trip setting .
- Trip output CONV_IFLT 5 V clamped signal goes to Inverter Control ASIC for pull out of CONV_ON signal that comes back through a buffer as CONV_EN signal to Converter control ASIC

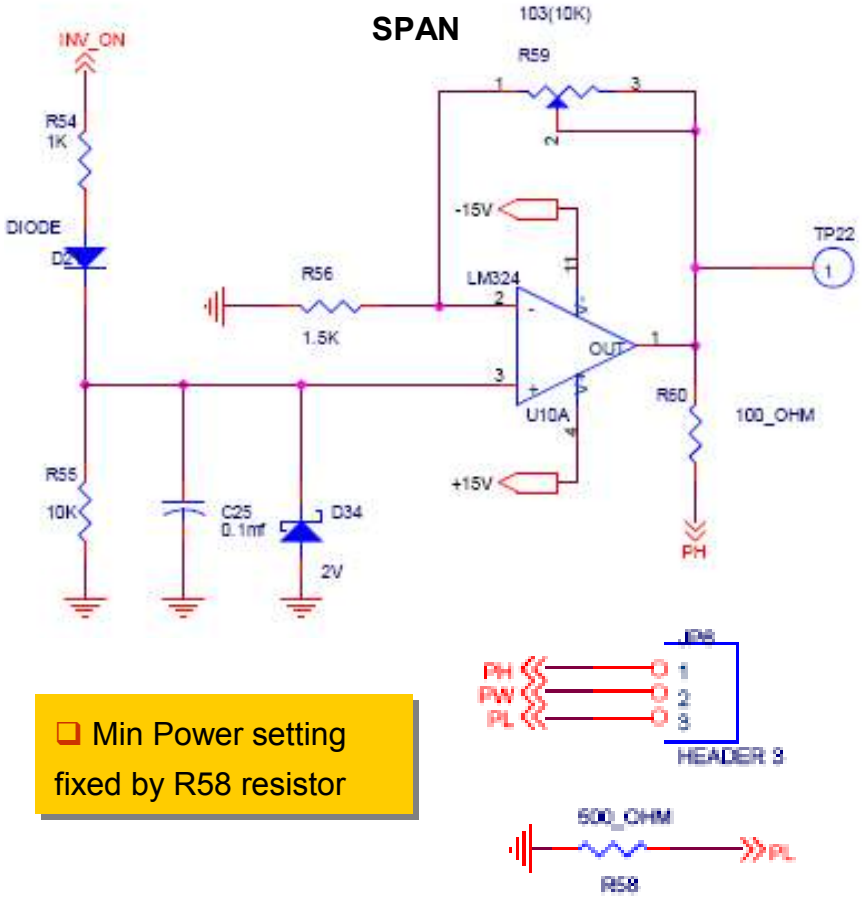
Circuit design notes – 6

- Inverter On signal and Power Control Pot supply
  - Feed back of actual power level from DC current through DCCT .
  - Inverter On signal allows Power pot reference – PH pin of Power set Pot .
  - PH (Pot HI pin) setting maximum adjusted with SPAN pot (R59) to adjust maximum power level depending on DCCT calibration .





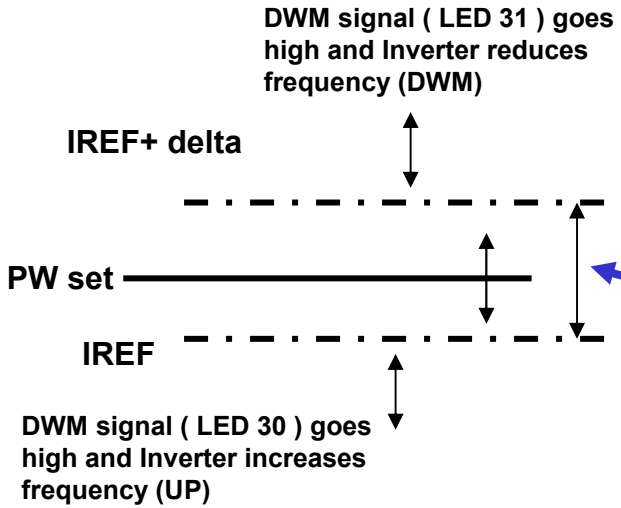
- Connect to DC bus through 200 K , 5 W resistor for Pos and Neg

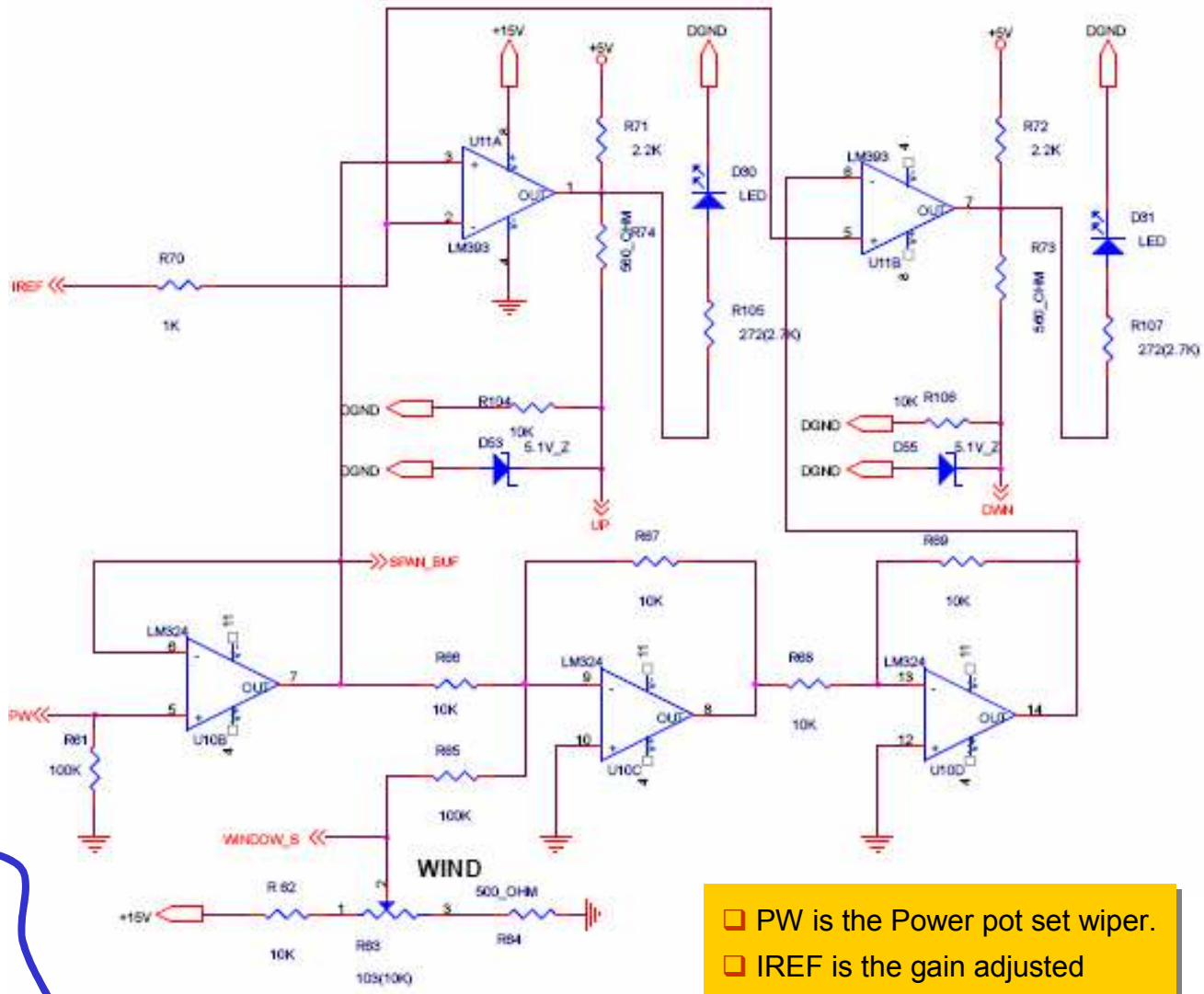


- Min Power setting fixed by R58 resistor

Circuit design notes – 7

- Inverter Power Control using Frequency UP and DWN SIGNAL .
  - Feed back of actual power level IREF.
  - Power set voltage PW from Power pot wiper .
  - WIND setting (R63) sets a small window above IREF (IREF plus delta)
  - PW within Window locks frequency



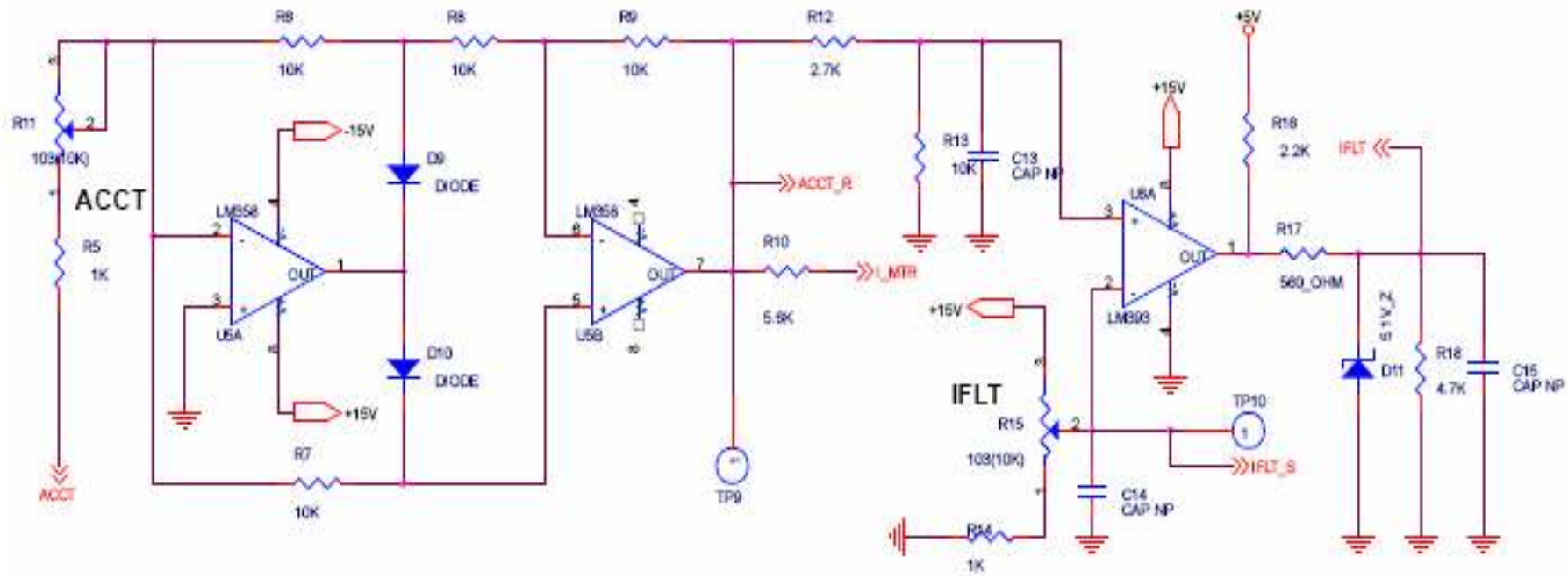


WINDOW

- PW is the Power pot set wiper.
- IREF is the gain adjusted DCCT signal proportional to power

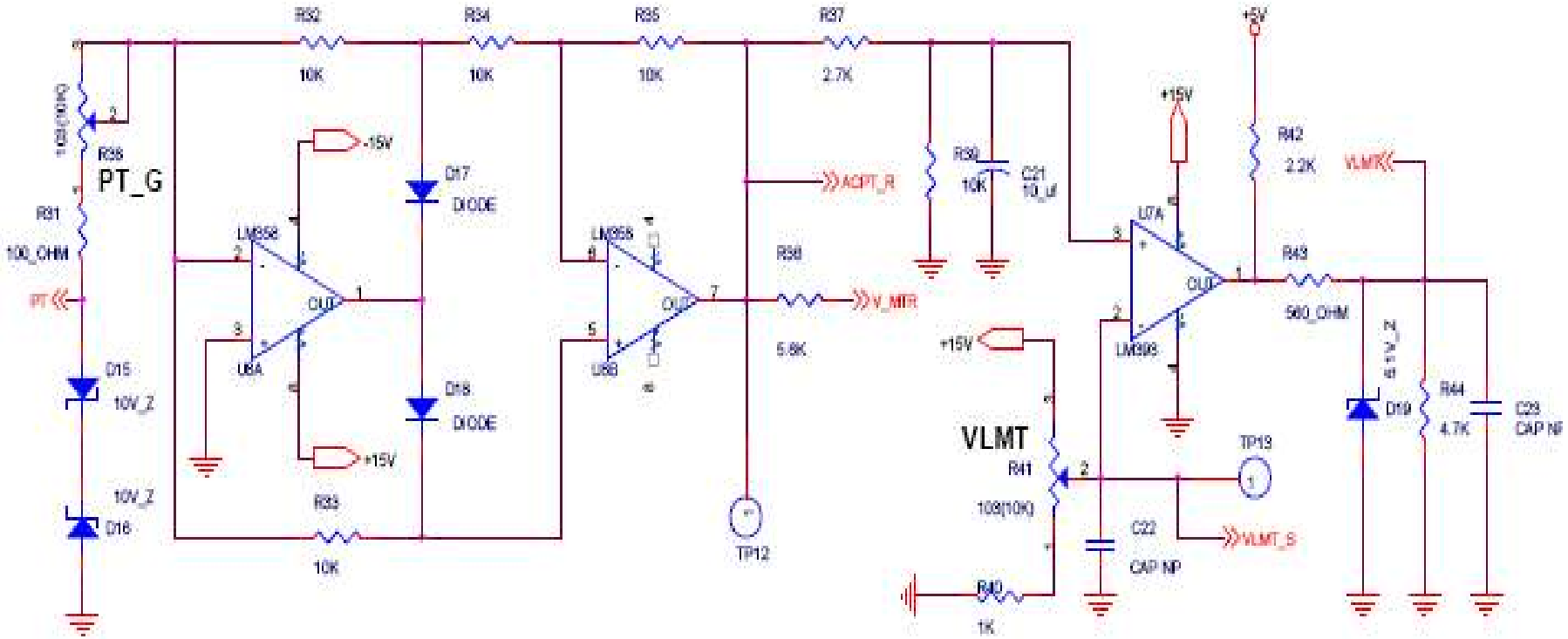
Circuit design notes – 8

- Inverter Trip setting (IFLT)
  - Feed back of Inverter current from medium Frequency CT – ACCT.
  - TP9 is full wave precession full wave rectified MF current waveform .
  - Compared at Comparator U6A for IFLT setting (R15) . Unit trips on Inverter Overcurrent when this IFLT is sensed.



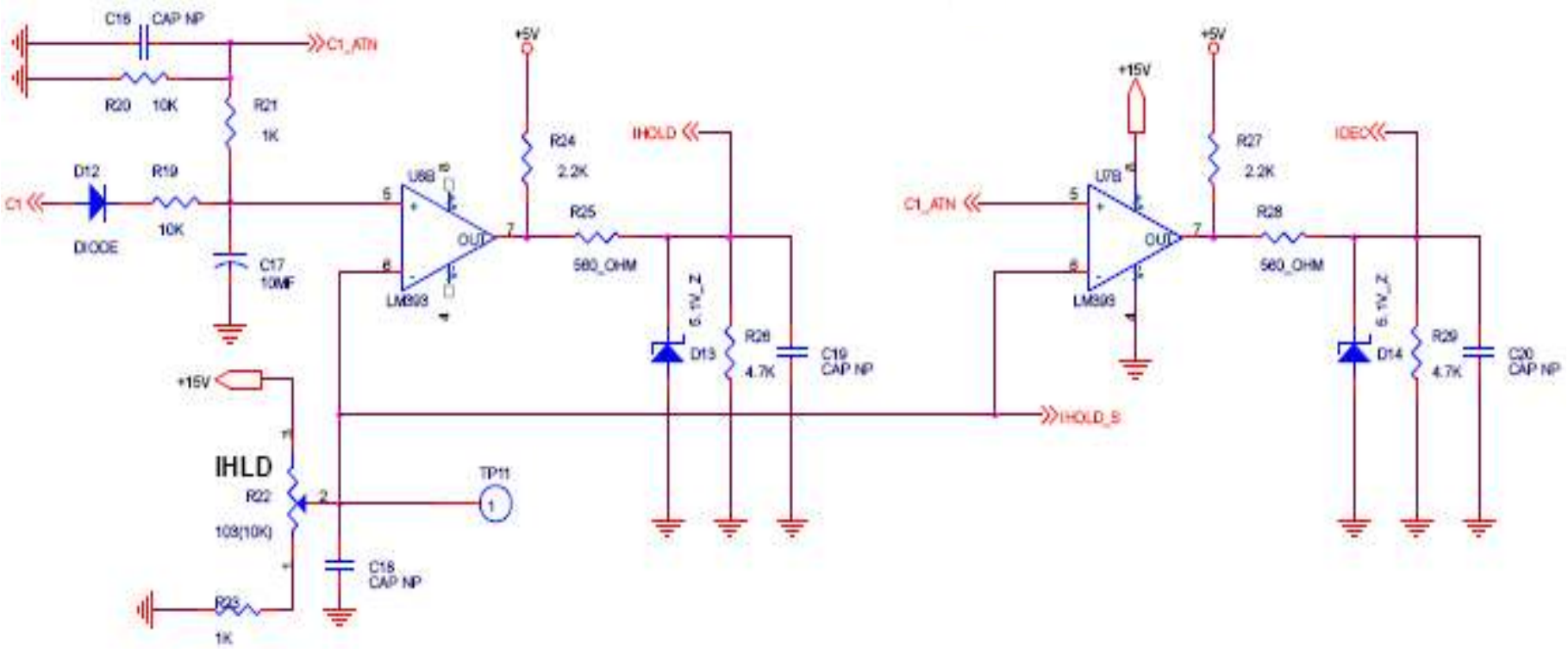
Circuit design notes – 9

- Inverter Limit setting (VLMT)
  - Actuated by Volt limit (VLMT) pot R41.
  - PT feedback for Inverter Volt sensing . Precession rectifier for full wave rectification .
  - PT gain adjustment (PT_G) R38.
  - Inverter frequency control overrides Power pot setting and goes to HOLD state .



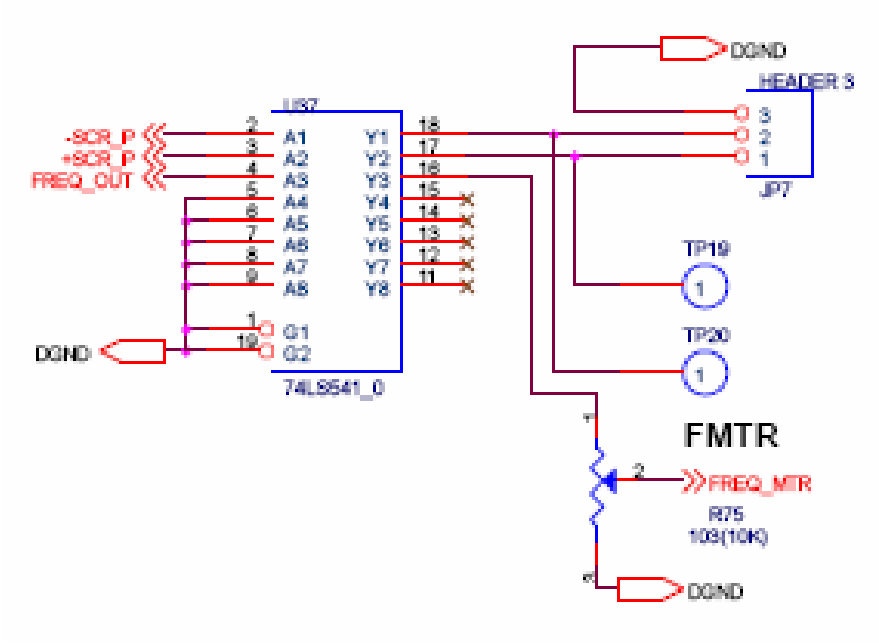
Circuit design notes – 10

- External Power hold facility (HOLD)
  - Used when Dual track configuration is used . Two Inverters working on common DC bus and each inverter power under hold limit when other inverter is in high power (Needs auxiliary Current summation card linked to DCCTs in both inverter DC use bus bar)
  - Signal C1 compared with HOLD pot (R22) and IHOLD signal is produced.
  - C1 attenuated signal (10 % attenuation) is compared with HOLD set IHLD and IDEC actuated . This is a feature when the second unit in dual track can be auto reduced in power ..



Circuit design notes – 11

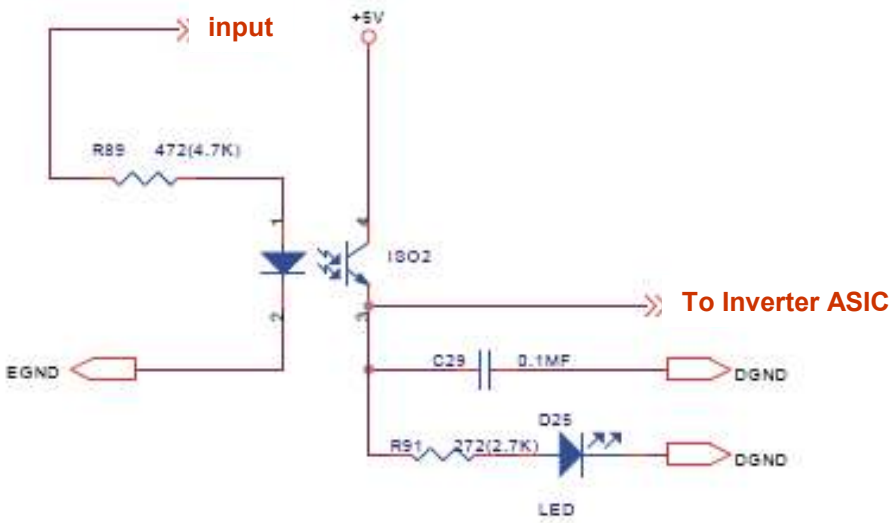
- Frequency meter calibration
  - Inverter ASIC provides a pulse train of double the inverter frequency with fixed on time and variable off time . As frequency goes up , off time drops and so duty cycle effectively increases. This is Buffered and a adjustment pot (R75) FMTR is provided to directly link to a 1 mA fsd frequency meter .



Circuit design notes – 12

- External interlocks for water system and control
  - Breaker on sense - To allow converter to be turned on sensing MCCB on . ***(LED D42)***
  - Phase sequence sense – IF activated , unit will not start (wrong phase sequence) . Need to use external Phase sequence relay . By pass if not used. ***(LED D47)***
  - ON sense - connected to Power ON push button to start inverter . ***(LED D29)***
  - OFF sense – Connected to Power OFF push button which is also fault reset . ***(LED D28)***
  - RAWPR sense – Raw water pressure low sensing . High when Pressure is normal ***(LED D27)***
  - GLD sense - Ground detector – High when Ground detector senses earth fault from an external ground detector. ***(LED D28)***
  - DMPR – DM water pressure low sensing . High when Pressure is normal . ***(LED D25)***
  - DMTMP – DM water temperature sensing . High when temperature is normal. ***(LED D24)***

- All external interlocks and actuations through Opto couplers



Power up sequence .

- Power up sequence
  - Breaker on - (when Units have Thyristors front end converters) .
  - Checks if phase sequence is alright and no water fault (Interlock lamps D42,47,227,26,25,24 will glow).
  - DC fault may light up . Press RESET (OFF PB) to reset DC fault .
  - Ready lamp blink will indicate that inverter is ready for start up.
  - Press Power ON (ON PB)
  - Inverter should start up at lowest frequency (approx 30ᴗ . .z)
  - At lowest pot setting , Inverter would continue running at lowest power setting . (D31 LED in control card would glow if DCCT calibration is correct . Else Unit will go up gradually in frequency and power till actual power sensed through DCCT is near Pot setting .
  - Increase POWER POT to raise frequency and power . When Power raises LED D30 in control board will light up momentarily as the frequency rises.
  - When Power reaches pot setting , frequency will lock .
  - Power OFF will stop the Unit.
  - In case of any fault , the appropriate fault lamp will go on and inverter stop.
  - During a fault indication the REDY lamp on front facia will glow permanently . Will go back to normal blink state when fault is reset .
  - Note that in case of GLD (Ground fault) I-over current indication and DCFLT indicator could also turn on depending on nature of GND fault.